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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,929	07/07/2003	Shigeyuki Aino	Q76416	6920

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EXAMINER	
MEHRMANESH, ELMIRA	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 03/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/612,929	AINO ET AL.	
	Examiner	Art Unit	
	Elmira Mehrmanesh	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The application of Aino et al., for an "Information processing apparatus" filed July 7, 2003, has been examined.

Claims 1-18 are presented for examination.

Information disclosed and listed on PTO 1449 has been considered.

Claims 1-18 are rejected under 35 USC § 102.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Horst et al. (U.S. Patent No. 5,751,932).

As per claim 1, Horst discloses an information processing apparatus (col. 10, lines 29-32) comprising:

First and second computer elements (Fig. 1A, elements 12A, 12B) which execute the same instructions substantially simultaneously and which are substantially synchronized with each other (col. 16, lines 19-25)

A first memory element which is provided in said first computer element and which is read and written by said first computer element during a first state (Fig. 2, element 28)

A second memory element which is provided in said first computer element and which is written by said second computer element during the first state (Fig. 2, element 22, and col. 85, lines 31-44)

And a control element which makes said first computer element read from said second memory element during a second state (Fig. 2, elements 26a, 26b).

As per claim 2, Horst discloses said control element makes said first computer element write to said first and second memory element during the second state (col. 88, lines 10-21).

As per claim 3, Horst discloses said control element copies the contents of said second memory element to said first memory element during the second state (col. 85, lines 31-44 and col. 88, lines 10-21).

As per claim 4, Horst discloses said control element copies the contents of said second memory element to said first memory element during the second state in parallel with the read or write access process to said second memory element (col. 13, lines 6-12).

As per claim 5, Horst discloses said control element copies the contents of said second memory element to said first memory element unless the access is present (col.

41, lines 48-67).

As per claim 6, Horst discloses said second state is when said first memory element has uncertainty (col. 91, lines 1-5).

As per claim 7, Horst discloses said second state is when said first memory element is updated (col. 71, lines 37-41 and col. 91, lines 34-37).

As per claim 8, Horst discloses said second state is when said first computer element is rejoined to said second computer element (col. 91, lines 6-21).

As per claim 9, Horst discloses said first computer element further includes at least one processor (Fig. 2, elements 20a, 20b)

And wherein said control element creates, during said second state, a first route from said second memory element to said first processor in response to a read access request (Fig. 1B, elements 12A, 12B, 14A, 14B), a second route from said processor to said second memory element in response to a write access request and a third route from said second memory element to said first memory element unless said read access request and said write access request are present (col. 34, lines 26-40).

As per claim 10, Horst discloses an information processing apparatus (col. 10, lines 29-32) comprising:

First and second computer elements (Fig. 1A, elements 12A, 12B) which execute the same instructions substantially simultaneously and which are substantially synchronized with each other (col. 16, lines 19-25)

A first memory area which is provided in said first computer element and which is written by said first computer element during a first state (Fig. 2, element 28)

A second memory area which is provided in said first computer element and which is read and written by said second computer element during the first state (Fig. 2, element 22, and col. 85, lines 31-44)

And a control element which makes said first computer element read from said second memory area during a second state (Fig. 2, elements 26a, 26b).

As per claim 11, Horst discloses said control element makes said first computer element write to said first and second memory area during the second state (col. 88, lines 10-21).

As per claim 12, Horst discloses said control element copies the contents of said second memory area to said first memory area during the second state (col. 85, lines 31-44 and col. 88, lines 10-21).

As per claim 13, Horst discloses said control element copies the contents of said second memory area to said first memory area during the second state in parallel with

the read or write access process to said second memory area (col. 13, lines 6-12).

As per claim 14, Horst discloses said control element copies the contents of said second memory area to said first memory area unless the access is present (col. 41, lines 48-67).

As per claim 15, Horst discloses said second state is when said first memory area has uncertainty (col. 91, lines 1-5).

As per claim 16, Horst discloses said second state is when said first memory area is updated (col. 71, lines 37-41 and col. 91, lines 34-37).

As per claim 17, Horst discloses said second state is when said first computer element is rejoined to said second computer element (col. 91, lines 6-21).

As per claim 18, Horst discloses said first computer element further includes at least one processor (Fig. 2, elements 20a, 20b)

And wherein said control element creates, during said second state, a first route from said second memory area to said first processor in response to a read access request (Fig. 1B, elements 12A, 12B, 14A, 14B), a second route from said processor to said second memory area in response to a write access request and a third route from

said second memory area to said first memory area unless said read access request and said write access request are present (col. 34, lines 26-40).

Related Prior Art

The following prior art is considered to be pertinent to applicant's invention, but nor relied upon for claim analysis conducted above.

Sonnier et al. (U.S. Patent No. 5,574,849), "Synchronized data transmission between elements of a processing system".

Sonnier et al. (U.S. Patent No. 5,751,955), "Method of synchronizing a pair of central processor units for duplex, lock-step operation by copying data into a corresponding locations of another memory".

Horst (U.S. Patent No. 5,838,894), "Logical, fail-functional, dual central processor units formed from three processor units".

Horst et al. (U.S. Patent No. 6,233,702), "Self-checked, lock step processor pairs".

Huang et al. (U.S. Patent No. 5,398,331), "Shared storage controller for dual copy shared data".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elmira Mehrmanesh whose telephone number is (571) 272-5531. The examiner can normally be reached on 8-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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